Energy Efficient QAM Modulation/Demodulation Architecture using Reversible Logic Gates

Naveen K B, M N Sree Rangaraju

Abstract— Modulation scheme is one of the digital communication frameworks and most broadly utilized basic structures part including vast measure of complex calculations. It chooses the execution and power utilization of the digital communication framework. Hence forth in this paper defines novel low power architectures for Quadrature Amplitude Modulation (QAM) schemes are accomplish in view of the reversible logic gates because of its low power utilization as a result of balanced correspondence between the info and yields. Significance of the gate level advancements will be represented to lessen the force utilization of the QAM adjustment frameworks. Datapath architectural advancements for reversible logic gates are executed to accomplishing insignificant power utilization. Diverse low power reversible datapath segments such as adder and multiplier are intended to diminish the power utilization of the for QAM modulator frameworks. The qam modulators were digitally demonstrated in verilog HDL coding and combined utilizing rhythm RTL compiler with 65nm mechanical library hub. A correlation between cutting edge existing reversible logic and proposed reversible logic architectures has been made. The proposed low power reversible datapath architectures have decreased power utilization of the QAM regulation frameworks when contrasted with existing reversible logic frameworks.

Index Terms— QAM, Modulator, Demodulator, HDL Coding, Low power, Reversible Logic, Multiplier, Feynman Gate, HNG Gate

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1 INTRODUCTION

Digital Modulation and Demodulation schemes are the distinct building blocks in digital communication system. The achievement of power optimizations is concerned in reversible logic implementations. Modulators and demodulators are the subsystems of digital communication system [1]. Digital data is represented by exhaustible number of digital signals and it has finite number of periods and each periods are encodes in equal number of digital bits. QAM techniques can be extending to implement the modulation and demodulation schemes. In the emerging technology and due to advancement in scaling, portable devices are increase in demand. Power optimization will become more complexity in portable electronic devices. Thus low power QAM modulator and demodulator are expound by consider the data values inside the memory as per the design data. Implementation of QAM is done by considering algorithm optimizations using reversible logic gates in reduction of power consumption because of one to one mapping in nature [2]. QAM digital scheme will convey the information of two digital bits of data and modeling the amplitude of two carrier digital signals by considering quadrature components [3]. QAM was used broadly in digital telecommunication system. As the design quality of digital system is enhanced and this leads in complexity in integrated circuits, then the transistors in integrated circuits are increased their numbers to achieve high speed in clocking frequency thus the complexity increases in digital system which leads to increase in power consumption. The conventional logic are irreversible in nature, it dissipates to a greater extent of heat and this rise in loss of information in every bit transactions. The information will erase due to energy loss and information losses cannot recover back in conventional logic [4]. Hence we can get the better of these problems by considering the circuit design based on reversible logic gates in standard level of integration in fabrication process because of its one to one mapping and hence output can be defined by input and vice versa [5]. In this paper we have con-

sider and developed (TYPE I design) reversible logic based QAM architecture and further novel architectures are optimized using reversible logic gate to reduce power in proposed QAM architecture (TYPE II design).

The other sections of the paper are organized as follows. Section 2 describes the importance of reversible logic, section 3 describes quadrature modulation schemes, Section 4 describes the digital implementation of QAM modulation/demodulation realizations, section 5 gives the results of QAM in TYPE I and TYPE II methodology and section 6 concludes the work.

2 REVERSIBLE LOGIC

Reversible Logic outline is one of rising range in the research field and it has applications in quantum, optical, CMOS and nano advancements. Subsequently reversible logic frames an immaculate suit on account of its great low power scattering. Bennett shows zero power dissipation can be done by using reversible logic [5]. Reversible rationales create remarkable yield vectors from the info vectors and the other way around with the goal that they can have coordinated correspondence between the information and yields. Commonly reversible logic gate comprises of k-inputs and k-outputs (number of inputs are equal to number of outputs), which yields in example to produced by mapping in every conceivable info design [6]. The Reversible Logic Circuits are a kind of novel circuits that can maintain a strategic distance from the data misfortune and vitality dispersal by the executing reversible logic operations [7]. Additionally, quantum PCs embrace the component of quantum mechanics, and destined to comply with the quantum physical law, which can be a powerful answer for the disappointment of established physical law. Likewise, reversible logic amalgamation has a nearby connection with quantum logic combination, and the strategy for reversible logic union can be utilized to actualize quantum logic blend, thus in this

way the investigation of reversible logic amalgamation will add to the advances in the related examination fields, including outline of the ultra-low power IC and quantum processing. Be that as it may, the speculations, strategies and devices of reversible logic amalgamation are a long way from all around created. In view of the amalgamation many-sided quality and the absence of learning and involvement in the field, the vast majority of these techniques are insufficient development and insufficient consider numerous blend targets at the same time. A few Reversible Logic Gates such as Feynman Gate, Peres Gate, HNG Gate and Toffoli Gates are utilized in the QAM modulation and demodulation work [8].

3 QUADRATURE AMPLITUDE MODULATION

3.1 Digital QAM Modulation

The inspiration for QAM originates from the way that a DSBSC signal involves double the transmission capacity of the message from which it is determined. QAM re-establishes the equalization by setting two autonomous DSBSC, got from message #1 and message #2, in the same range space as one
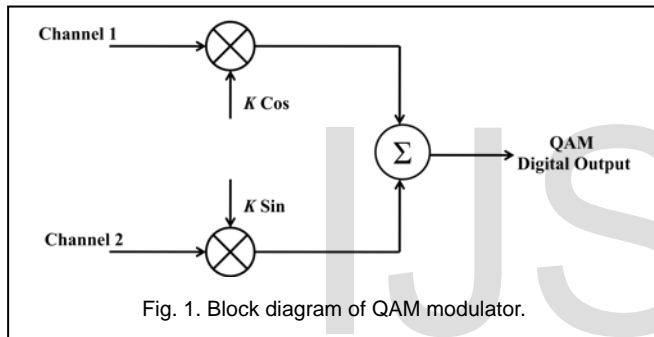

Fig. 1. Block diagram of QAM modulator.

DSBSC. it is utilized due to its transmission capacity saving properties and it is not utilized for multiplexing two autonomous messages. In given information double arrangement (message) at the rate of n bit/s, two successions might be acquired by part in terms of the bit stream into two ways and each of n/2 bit/s. This is same as a serial-to-parallel change. The two streams turn into the channel 1 and channel 2 messages of figure 1. In light of the split rate the bits in I and Q ways are extended to double the info arrangement bit clock period. The two messages are recombined at the collector, which utilizes a QAM-sort demodulator. The regulation plan in which two orthogonal transporter signs are utilized to balance over the physical channel is called QAM [9]. The transporter sign is changed (in both sufficiency and stage) as indicated by the info information signal in the QAM technique and all is said in done, two orthogonally distinctive transporter inputs are picked.

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3.2 Digital QAM Demodulation

In the QAM demodulator framework, the QAM balanced sign is bolstered as information and increased with both in eliminate and of stage transporter frequencies to create I and Q signals which are then separated and further prepared. The QAM modulator is so named on the grounds that, in simple applications, the messages do in certainty shift the adequacy of each of the DSBSC signals.

Every message has just two levels, ±v volt. For a non-band-constrained message this doesn't vary the sufficiency of the yield DSBSC. as the message changes extremity this is trans-
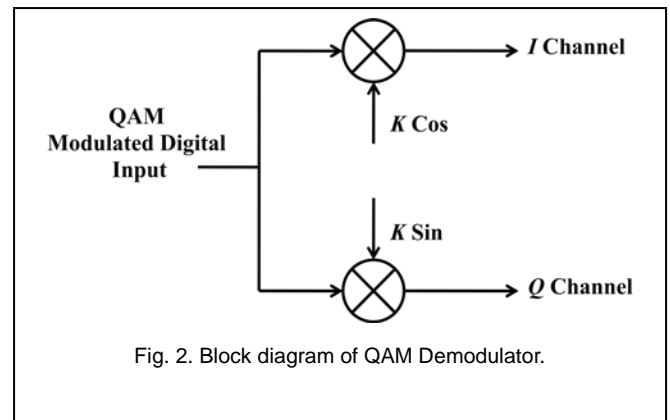

Fig. 2. Block diagram of QAM Demodulator.

lated as a 180 stage shift, given to the DSBSC. Subsequently the sign in every arm is said to experience a 180 stage move, or stage shift keying or PSK. Since there are two PSK signals consolidated, in quadrature, the two channel modulator offers ascend to a quadrature stage shift keyed QPSK signal.

4 DESIGN AND IMPLEMENTATION

4.1 QAM Modulator

In the architecture of Quadrature Amplitude Modulation (QAM) technique, the digital data is given to the multiplier as shown in figure 1, which multiplies the amplitude and phase of the digital carrier signal as shown in figure 3 and these two carrier digital wave signals are considered in orthogonal to each other.. QAM modulation mechanism is considered for high speed digital signals, here signals are in 90° phase shift and hence the components are quadrature in nature [3]. In QAM, in-phase signal and a quadrature phase signal are modulated with a precise number of digital signals and then added.The QAM modulator consists of two multipliers & one adder as shown in figure 3. The input data is multiplied with imaginary & real part of carrier signals. Finally both the in phase & out of phase modulated signals are added to generate the QAM output. All the datapath components are implemented using Reversible Logic architecture to reduce power consumption.The figure 3 shows the 8X8 Braun array multiplier which is designed by reversible logic gates such as Toffoli gate, Peres gate and HNG gate. The 16-bit required output is obtained by multiplying two 8-bit inputs [10]. The figure 4 shows 16-bit QAM modulator design consists of 8*8 Braun array multiplier and 15-bit adder circuits [11]. QAM modulation architecture consists of two sinusoidal carrier signal such as Kcos and Ksin as expressed in general equation (1) and (2).

$$K \cos = \cos(2\pi f_c t) \qquad (1)$$

$$K \sin = \sin(2\pi f_c t) \qquad (2)$$

These two signals are orthogonal to each other with 90^0 phase shift. The input channel digital signals are multiplied with
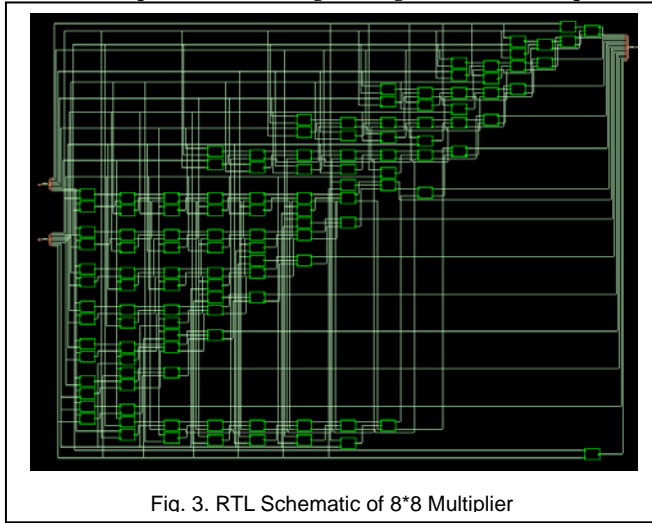

Fig. 3. RTL Schematic of 8*8 Multiplier

carrier digital signals to get QAM output. In the proposed work we considered 8-bit data length of the channel 1 and channel 2 and 8-bit data length of carrier digital signals such as Kcos and Ksin.
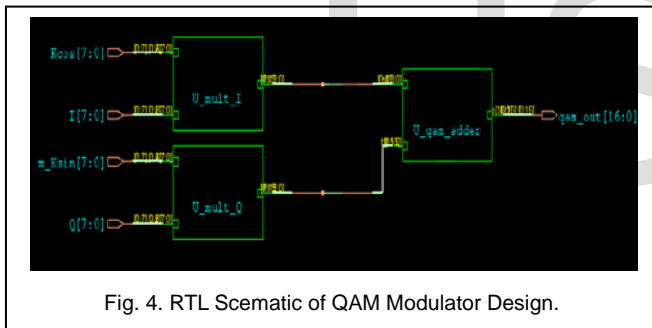

Fig. 4. RTL Scematic of QAM Modulator Design.

Hence in the architecture of QAM modulator consists of two 8*8 multipliers and one 16-bit adder [12]. The 8-bit digital input channels (Channel 1 and Channel 2) data is multiplied with imaginary and real part of 8-bit digital carrier signals i.e. Kcos phase and Ksin (m_Ksin) phase to get 16-bit 'I' (In-Phase) and 16-bit 'Q' (Quadrature-Phase) channels. Finally both in-phase and quadrature-phase digital signals of the QAM architecture are added together using 16-bit adder circuit to generate the 17-bit QAM modulation output [13]. All the datapath components are implemented using reversible logic gates in QAM modulation architecture to reduce power consumption.

4.2 QAM Demodulator

TheThe QAM demodulator consists of two multipliers. The input modulated data is multiplied with imaginary & real part of carrier signals to generate in phase & out of phase signals. Both the multipliers are implemented using Reversible Logic architecture to reduce power consumption. QAM demodulator architecture as shown in figure 4, here the QAM modulated digital signal is fed as an input and multiplied with

both in-phase and quadrature-phase carrier digital frequency bits to generate I and Q signals [14]. The QAM demodulator architecture is implemented using CADENCE tool in 65nm technology as shown in figure 5. The architecture consists of 17-bit QAM modulator block and two 17*17 Braun array multipliers block design. In the QAM demodulator design we considered 17-bit data of Kcos and Ksin, hence the multiplier which acts as a mixer to mix the 17-bit QAM modulated digi-
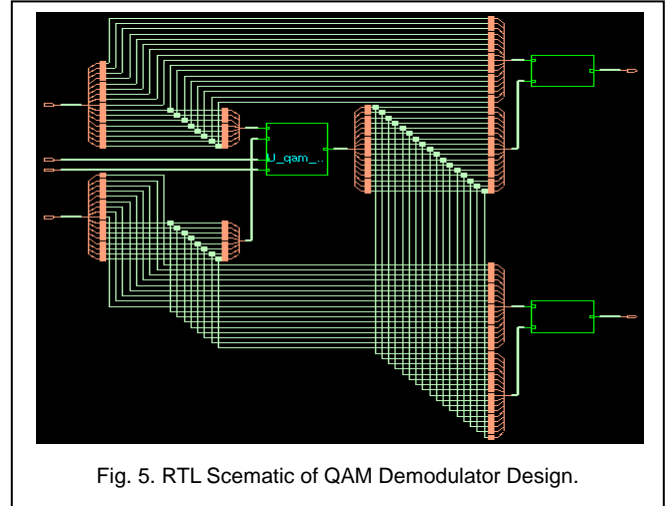

Fig. 5. RTL Scematic of QAM Demodulator Design.

tal signals with 17-bit Kcos (Imaginary) and 17-bit Ksin (Real) digital carrier signal to generate 34-bit 'I' (In-Phase) and 34-bit 'Q' (Quadrature-Phase) channels and all the data path architecture such as QAM modulator design and multiplier design are optimized by using reversible logic gates for low power design.

5 RESULTS AND DISCUSSIONS

Designs of QAM Modulator/Demodulator architectures have been illustrated and designed in 65nm technology for low power digital communication applications. Digital circuit designs have been modeled using reversible logic gates in HDL coding and

TABLE 1
ANALYSIS OF QAM MODULATOR DESIGN

Design	Parameter	(TYPE I) Reversible Logic Implementation for Conventional Logic Design	(TYPE II) Proposed Reversible Logic Design
QAM Modulator	Leakage power	31.939 µW	22.773 µW
	Delay	3.286 ns	4.034 ns
	Area	2974 µm²	2974 µm²

Statements µW= micro Watt, ns = nano second, µm= micro meter

TABLE 2
ANALYSIS OF QAM DEMODULATOR DESIGN

Design	Parameter	(TYPE I) Reversible Logic Implementation for Conventional Logic Design	(TYPE II) Proposed Reversible Logic Design
QAM Modulator	Leakage power	173.802 µW	124.497 µW
	Delay	10.072 ns	11.575 ns
	Area	16169 µm²	16169 µm²

Statements µW= micro Watt, ns = nano second, µm= micro meter

verified its functionality using ModelSim simulator tool through the waveform editor. Conventional XOR gate is design based on AOI logic in TYPE II design and reversible logic gates such as Feynman gate, Peres gate, Toffoli gate and HNG Gates are used to design the combinational circuits in 65nm technology. The TABLE I and Table II gives the information of QAM Modulator and Demodulator of Type I and Type II designs.

The QAM modulation as shown in figure 6, output is obtained by considering the inputs of channel 1 and channel 2 with 8-bits each. The two 8-bit inputs are multiplied by Kcos and Ksin of 8-bit data to obtain 'I' phase (I_temp) and Q phase (Q_temp). 17-bit QAM modulator (qam_out) output is obtained by adding16-bit of in-phase and 16-bit of quadrature-phase data. 34-bit QAM Demodulator design is determined by considering the 17-bit QAM modulator digital output and it is multiplied with 17-bit of Kcos and 17-bit of Ksin such that the
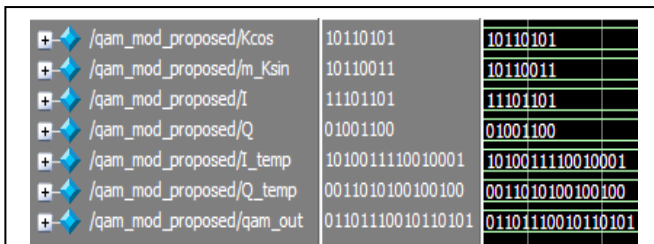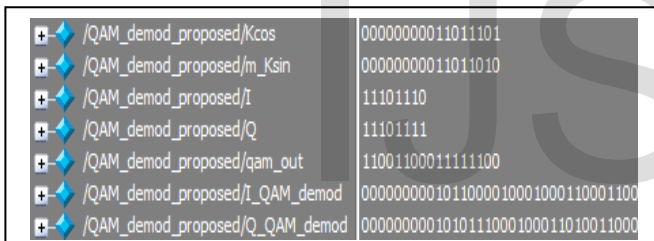

Fig. 6. QAM Modulator Simulation Results.

Fig.7. QAM Modulator Simulation Results.

two outputs defined as in-phase (I_QAM_demod) and quadrature-phase (Q_QAM_demod) are simulated as shown in figure 7. Hence QAM Demodulator output is achieved by using reversible logic gates.

6 CONCLUSION

The QAM modulator power consumption is reduced by applying the proposed concept on the multiplier & adder blocks. In the QAM demodulator block, the leakage power is minimized by optimizing the power consumption of multiplier block in Type II design. Most copiously used component of the QAM modulator/demodulator was optimized and its impact at the higher hierarchical level was observed. Low power datapath architectural optimizations are provided to the reversible logic architectures and applied to the QAM modulator design. During this study, it has been observed that the datapath architectural optimizations facilitate greater control over the design constraints and it also observed that the use of datapath optimizations can be extended to any bit-width QAM modulator. The building block of QAM modulator leakage power is optimized by 33.50% and QAM demodulator by

33.05% optimization of reversible logic design in TYPE II reversible logic design when compared to TYPE I reversible logiv design respectively. In this paper novel low power architectures for various modulation & demodulation schemes such as QAM have been proposed & proven. The reversible logic based low power datapath (adder & multiplier) architectures were proposed for QAM modulator & demodulator. The results demonstrate the proposed value of power minimization. The proposed gate level architectures can be further optimized at transistor level. The reversible logic plays a pivotal role in digital circuits and reversible computing has wide spread applications in modern day electronic systems. The efforts reported in this research paper represent a strong contribution towards the advancement of design and synthesis reversible logic circuits for emerging technologies.

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